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VPX/FMC ADC & DAC Boards

Target Applications	Status	Ruggedized version	Model	Form Factor	Input (ADC)	Output (DAC)	Resolution (bits)	Sample rate	On board FPGA	Bandwidth	SNR (dBFS)	ENOB (bits)	SFDR (dBc)	SW Drivers	Comment	Firmware support
LIDAR, 3D Laser, High Energy Physics. May be used in EW and Wideband Radar.	Production	AS,AR,CS	AV101	3U VPX	1		10	10 GS/s	Virtex 6	> 3GHz	48 (1 GHz)	7.2 (1 GHz)	45 (1 GHz)	Win, Linux		Xilinx ISE 14.6 and later
Radar Emitter-Receiver. EW-ECM DRFM. Radar Target Simulator	Production	AS,AR,CS,CR	AV104	3U VPX	2	1	10 12	3 GS/s	Virtex 7	0.01 - > 4 GHz 0.01 - > 4 GHz	49 (2.6 GHz)	7.6 (2.6 GHz)	56 (2.6 GHz) 52 (2.6 GHz)	WIN, Linux	ADC to DAC latency < 26 ns @ 3 GS/s. Ultra low clock jitter < 150fs	Xilinx VIVADO 2015.2 and later
EW-ESM, RWR	Production	AS,AR,CS,CR	AV107	3U VPX	4		12	2.5 GS/s	Virtex 7	0.01 - > 5 GHz	58.5 (1 GHz)	> 9 @ 2.5GHz	69 @ 1 GHz. > 60 @ 2.5GHz	WIN, Linux	Optional DDC on ADCs. Individual clock synthesizer for each ADC with Fine Phase control. Build RWR 0-18GHz with 2 boards. Clock jitter of 60fs	Xilinx VIVADO 2015.2 and later
COMINT	Production	AS,AR,CS,CR	AV113	3U VPX	8		14	1.25 GS/s (AS). 1.1GS/s (AR, CS, CR)	Virtex 7	0.01 - >2.3GHz	65 @ 1 GHz	10.1 @ 1 GHz	> 65 @ 1 GHz	Win, Linux	Individual clock synthesizer for each Dual ADC with Fine Phase control. Build RWR 0-18GHz with 2 boards. Clock jitter of 60 fs	Xilinx VIVADO 2015.2 and later
Phased-Array - AESA Receiver. SAR Radar. EW-ESM RWR. LIDAR-LADAR	Production	AS,AR,CS,CR	AV121	3U VPX	4		12	4 GS/s	Virtex 7	0.01 - > 3.5GHz	54 (1 GHz)	> 8.6 @ 1 GHz	> 65 @ 1 GHz	WIN, Linux	Optional DDC on ADCs. Clock jitter of 60 fs.	Xilinx VIVADO 2015.2 and later
Phased-Array - AESA Receiver. SAR Radar. EW-ESM RWR, LIDAR-LADAR. MIMO	Production	AS,AR,CS,CR	AV122	3U VPX	8		14	3 GS/s	Kintex Ultrascale	>9 GHz	59 @ 1GHz	9.4 @ 1GHz	70 @ 1GHz	WIN, Linux	2 DDC per ADC with 2 - 48 decimation ratio with IQ Complex output	Xilinx VIVADO 2015.2 and later
Electronic Warfare – Electronic Attack. DRFM. Radar Transceiver. Target Simulator. Wideband Communication	Production	AS,AR,CS,CR	AV125	3U VPX	1	1	12	5.4 GS/s	Kintex Ultrascale	> 5.5 GHz > 6 GHz	55 @ 1GHz. 48 @ 2.1 GHz	8.5 @ 1GHz. 7.6 @ 2.1 GHz	56 (2.1 GHz) 60.5 @ 1 GHz	WIN, Linux	ADC to DAC latency < 34 ns for DRFM 2GHz Instantaneous BW	Xilinx VIVADO 2015.2 and later
Radar S-Band, C-Band and X-Band Transceiver. Radar Instrumentation. MIMO	Production	AS,AR,CS,CR	AV129	3U VPX	4	4	14 16	3 GS/s 6 GS/s	Kintex Ultrascale	2- >8 GHz 2- >8 GHz	57 @ 2.6GHz	9 @ 2.6GHz	70	WIN, Linux	2 DDC per ADC with 2 - 48 decimation ratio with IQ Complex output. All Ch phase coherent.	Xilinx VIVADO 2015.2 and later
	Development	AS,AR,CS,CR	AV134	3U VPX	8 / 4	2	12 16	5.2-10.4 GS/s 12.5 GS/s	Virtex Ultrascale+	> 8 GHz TBC	TBC	TBC	TBC	Win, Linux	Single ultralow jitter clock synthesizer. 2x 1G64 DDR4 SDRAM	
	Development	AS,AR,CS,CR	AV135	3U VPX	4		12	8-11 GS/s	Virtex Ultrascale+	> 18GHz	TBC	TBC	TBC	Win, Linux	Ultralow jitter (~ 40ps) clock synthesizer per ADC with fine phase control. 2x 1G64 DDR4 SDRAM	
	Development	AS,AR,CS,CR	AV138	3U VPX	4	4	12 14	5 GS/s 6.5 GS/s	RFSoC	TBC	TBC	TBC	~ 80 TBC	Win, Linux	Xilinx GEN1 and GEN3 ZYNQ UltraScale+ RFSoC ZU25DR/ZU27DR or ZU47DR	

ADC. EW-ESM. RWR. Radar Receiver. T&M.	Production	AS,AR,CS	AF202	FMC	2		12	1.5 GS/s		>2.3 GHz	57 (1 GHz)	8.9 (1 GHz)	60 (1 GHz)		Fully supported on ApisSys FMC carrier	VHDL cores for all HW
Arbitrary Broadband Signal Generation L, S and C bands for ATE, SDR, Radar Transmitter	Production	AS,AR,CS,CR	AF204	FMC		1	12	3 GS/s		> 5.5 GHz			52 (3.8 GHz)		Fully supported on ApisSys FMC carrier	VHDL cores for all HW
	Production	AS,AR,CS,CR	AF207	FMC		2	14	2.8 GS/s		> 5 GHz			67 (2.5 GHz)		5.6 GS/s with interpolator mode. Fully supported on ApisSys FMC carrier	VHDL cores for all HW
	Production	AS,AR,CS,CR	AF209	FMC		1	12	6 GS/s		> 7 GHz			50 (5 GHz)		Fully supported on ApisSys FMC carrier	VHDL cores for all HW
Arbitrary Broadband Signal Generation	Q2 '18	AS,AR,CS,CR	AF210	FMC		4	16	2.5 GS/s		> 1 GHz			TBD		Ultralow jitter on board clock (<100 fs). Supports Kintex UltraScale	VHDL cores for all HW

Versatile SBC Real time processing, EW, Radar, ATE	Production	AS,AR,CS,CR	AV108	3U VPX	Versatile SBC with FMC and XMC carriers				ZYNQ™ 7030/45 SoC					Linux	1 GB DDR3 SDRAM, 8 Gb NAND Flash, 2x GbE, USB2.0, HDMI, UART.	Xilinx VIVADO 2015.2 and later
Communication.	Production	AS,AR,CS,CR	AV109	3U VPX					Virtex 7					WIN, Linux		Xilinx VIVADO 2015.2 and later
Communication. Naval (data transmission from multiple sensors spread across ship)	Production	AS,AR,CS,CR	AV127	3U VPX	36x 10Gbps Optical Links. Full duplex				Kintex Ultrascale	14 Gbps per fiber				WIN, Linux	720 Gbps aggregate data throughput on Fibers. 1000 Gbps aggregate data throughput on commercial grade (14 Gbps per fiber)	
Chassis																
3U VPX 5 slots Open Frame Dev Chassis	Production	AS,CS,	AC101	3U Chassis	Open Frame - 5 slots Full Mesh backplane.										600 W PSU	Xilinx VIVADO 2015.2 and later
3U VPX 3 Slots Desktop Chassis	Production	AS	AC103	3U Chassis	Desktop - 3 slots OpenVPX										600 W PSU	Xilinx VIVADO 2015.2 and later
3U VPX 12 Slots Desktop Chassis	Production	AS	AC104	3U Chassis	19" - 5, 9 and 12 slots backplane										1200 W PSU	Xilinx VIVADO 2015.2 and later

Ruggedizing level as per VITA 47

AS = Air Standard (EAC4)

AR = Air Rugged (EAC6)

CS = Conduction Standard (ECC3)

CR = Conduction Rugged (ECC6)

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